IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT:	Herz et al.	**GROUP:**	Not yet assigned
SERIAL NO:	10/763,048	**EXAMINER:**	Not yet assigned
FILED:	January 22, 2004		
FOR:	STORAGE DEVICE FOR A MULTIBUS ARCHITECTURE		

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

PRELIMINARY AMENDMENT

Please amend the application as follows:

IN THE CLAIMS:

Cancel claims 11-19 and amend claims 3 and 5-9 as follows:

1.(Original) Storage device for a multibus architecture, comprising

– at least one memory (M) to store data (d), information and/or addresses,

– a memory connection (B) including a port (B0) to connect the memory (M) to a first bus (D0) of a multibus architecture (P, D0, D1, R),

– wherein the memory connection (B), the port (B0), and the first bus (P) have data lines (DL) to transmit the data (d), and, as required, transmit addresses (a) and/or control information to control the memory (M),

characterized by

– a switching device (SW, MTR, CU, ARB, MOD) to selectively connect the memory connection (B) to one of the buses (D1, P, R) for a memory access to effect transmission of data, addresses, and/or control information from or to this bus.